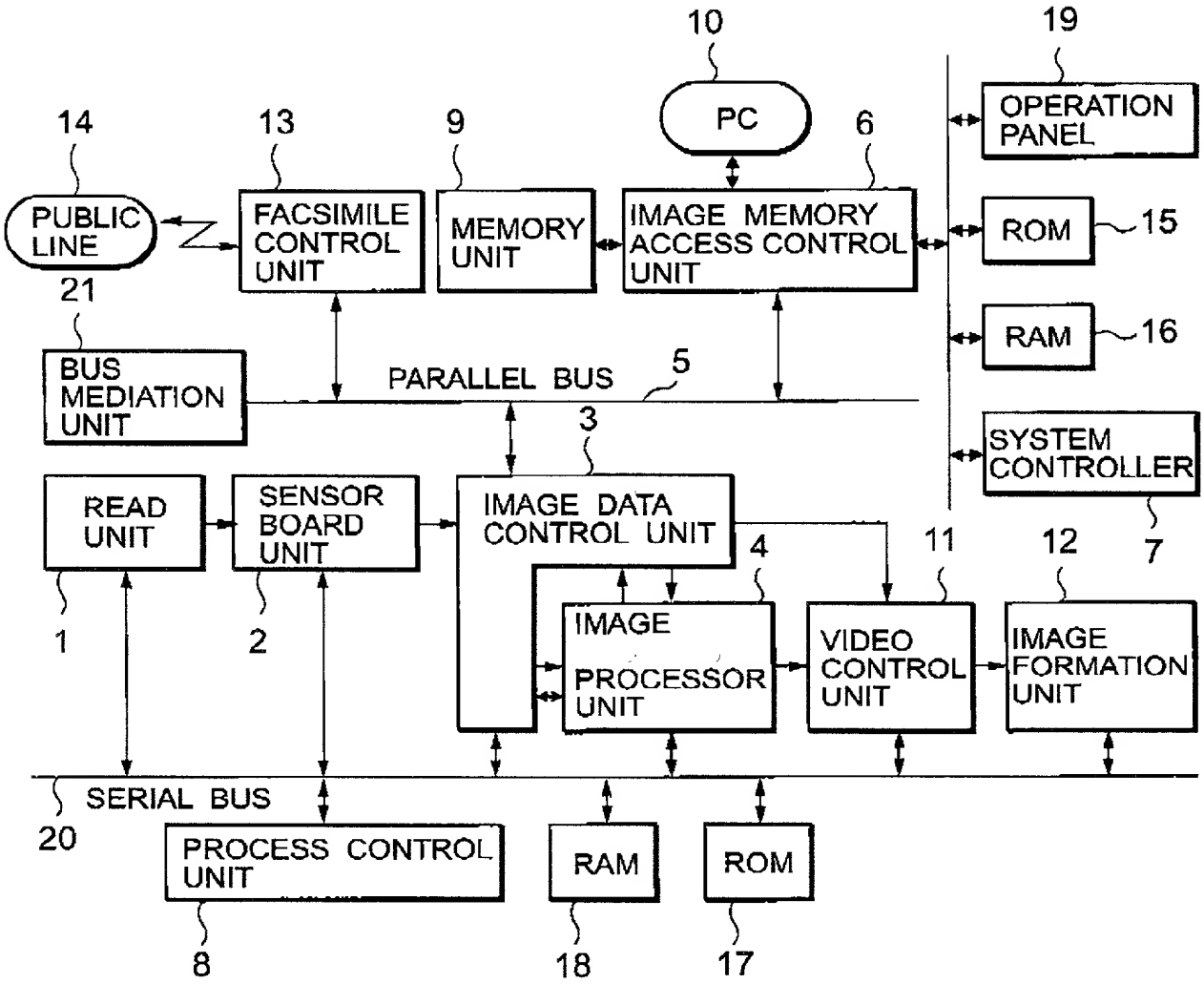

10
19
PC
OPERATION PANEL
14
13
9
6
PUBLIC LINE
FACSIMILE CONTROL UNIT
MEMORY UNIT
IMAGE MEMORY ACCESS CONTROL UNIT
ROM
15
21
RAM
16
BUS MEDIATION UNIT
PARALLEL BUS
5
3
SYSTEM CONTROLLER
READ UNIT
SENSOR BOARD UNIT
IMAGE DATA CONTROL UNIT
4
11
12
7
IMAGE PROCESSOR UNIT
VIDEO CONTROL UNIT
IMAGE FORMATION UNIT
1
2
SERIAL BUS
20
PROCESS CONTROL UNIT
RAM
ROM
8
18
17

FIG.1

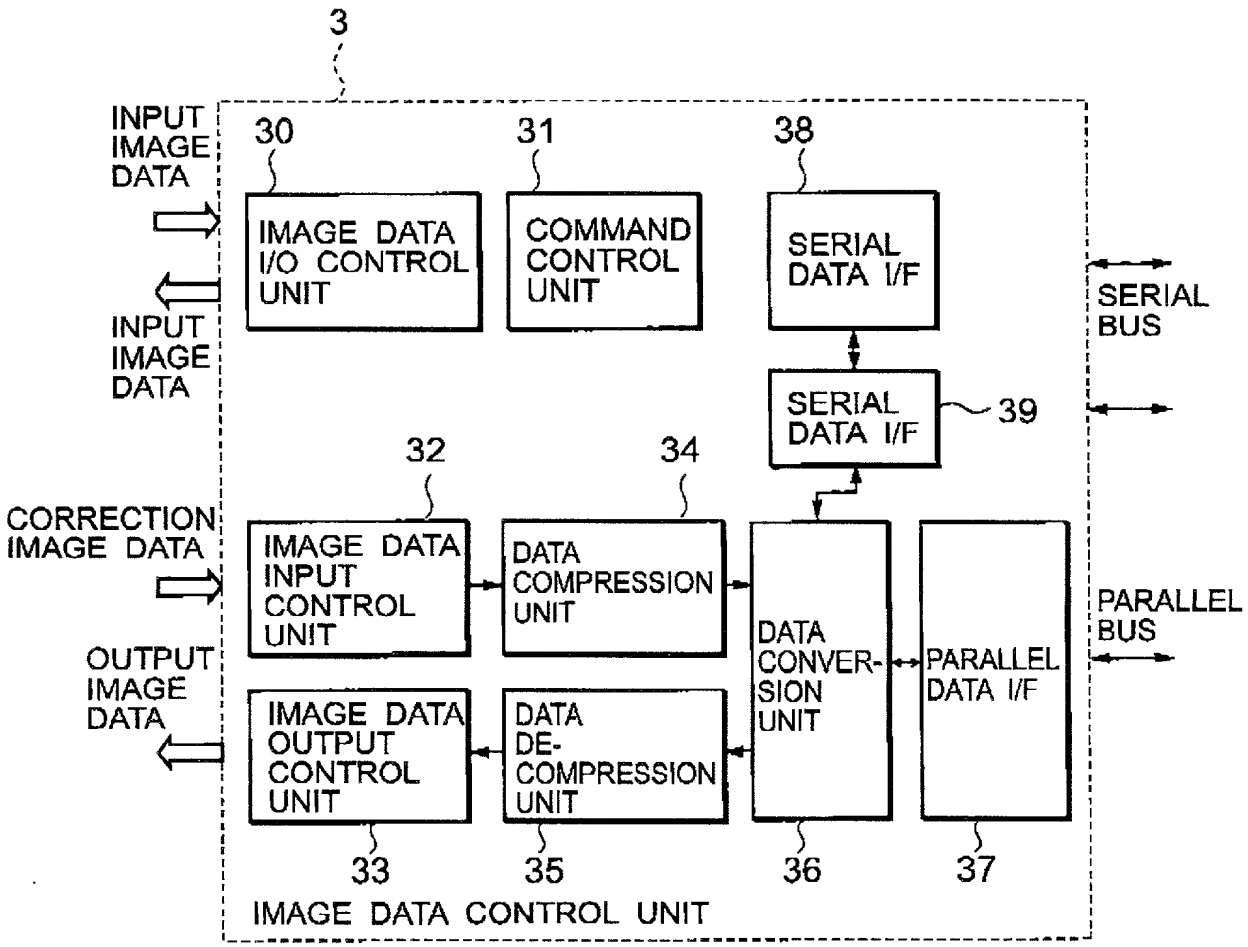

3
INPUT IMAGE DATA
30
31
38
IMAGE DATA I/O CONTROL UNIT
COMMAND CONTROL UNIT
SERIAL DATA I/F
SERIAL BUS
INPUT IMAGE DATA
SERIAL DATA I/F
39
32
34
CORRECTION IMAGE DATA
IMAGE DATA INPUT CONTROL UNIT
DATA COMPRESSION UNIT
DATA CONVER-SION UNIT
PARALLEL DATA I/F
PARALLEL BUS
OUTPUT IMAGE DATA
IMAGE DATA OUTPUT CONTROL UNIT
DATA DE-COMPRESSION UNIT
33
35
36
37
IMAGE DATA CONTROL UNIT

FIG.2

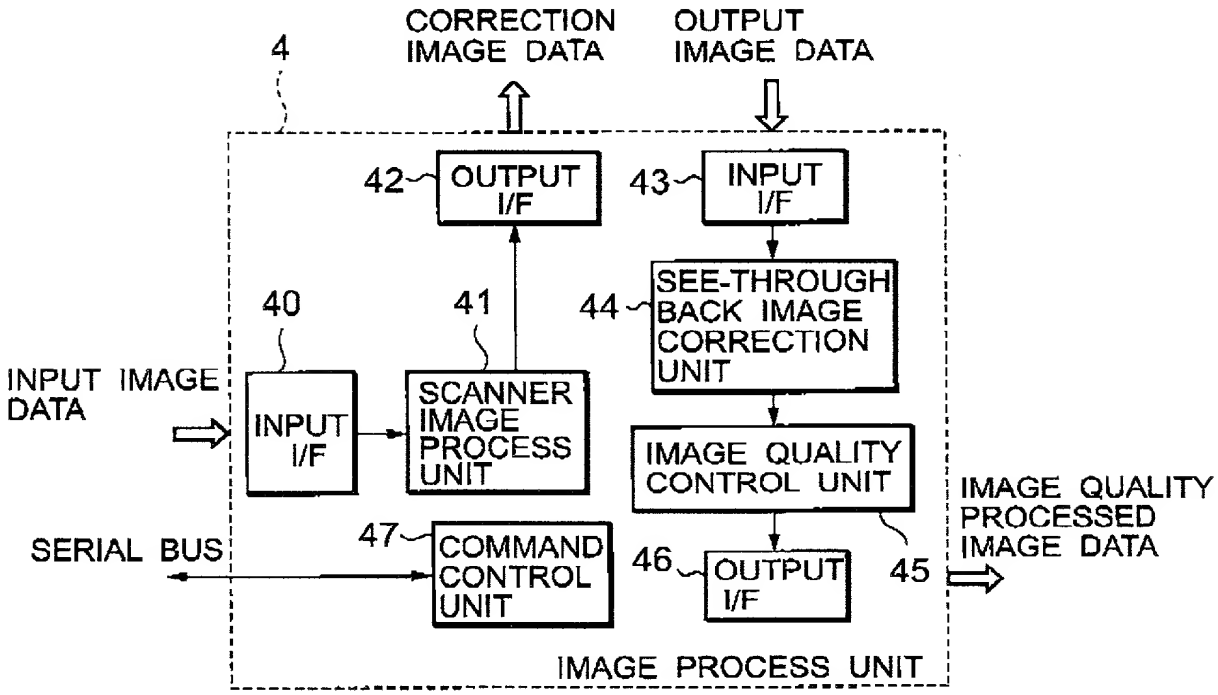

4
CORRECTION IMAGE DATA
OUTPUT IMAGE DATA
42
OUTPUT I/F
43
INPUT I/F
40
41
44
SEE-THROUGH BACK IMAGE CORRECTION UNIT
INPUT IMAGE DATA
INPUT I/F
SCANNER IMAGE PROCESS UNIT
IMAGE QUALITY CONTROL UNIT
IMAGE QUALITY PROCESSED IMAGE DATA
SERIAL BUS
47
COMMAND CONTROL UNIT
46
OUTPUT I/F
45
IMAGE PROCESS UNIT

FIG.3

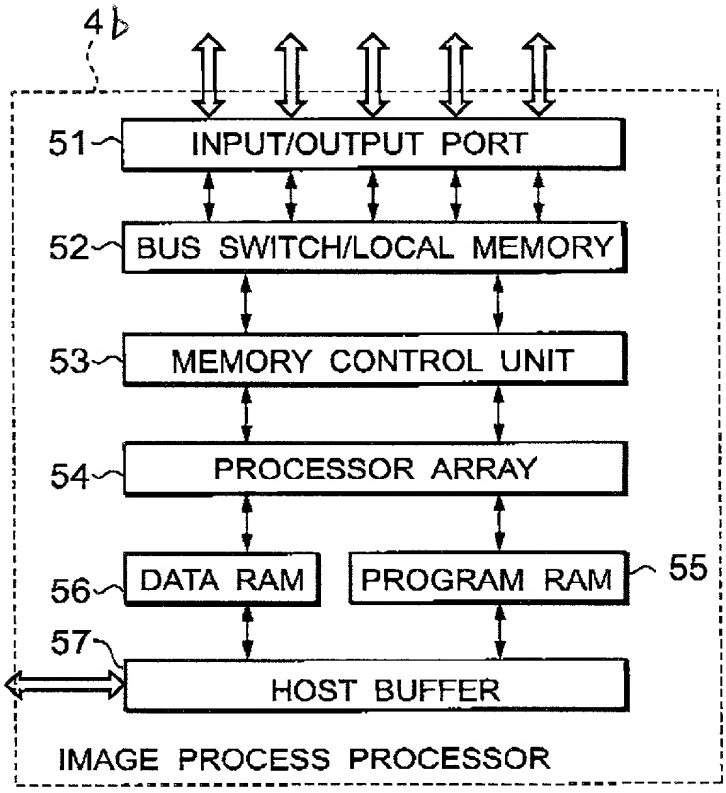

4b
51
INPUT/OUTPUT PORT
52
BUS SWITCH/LOCAL MEMORY
53
MEMORY CONTROL UNIT
54
PROCESSOR ARRAY
56
DATA RAM
PROGRAM RAM
55
57
HOST BUFFER
IMAGE PROCESS PROCESSOR

FIG.4

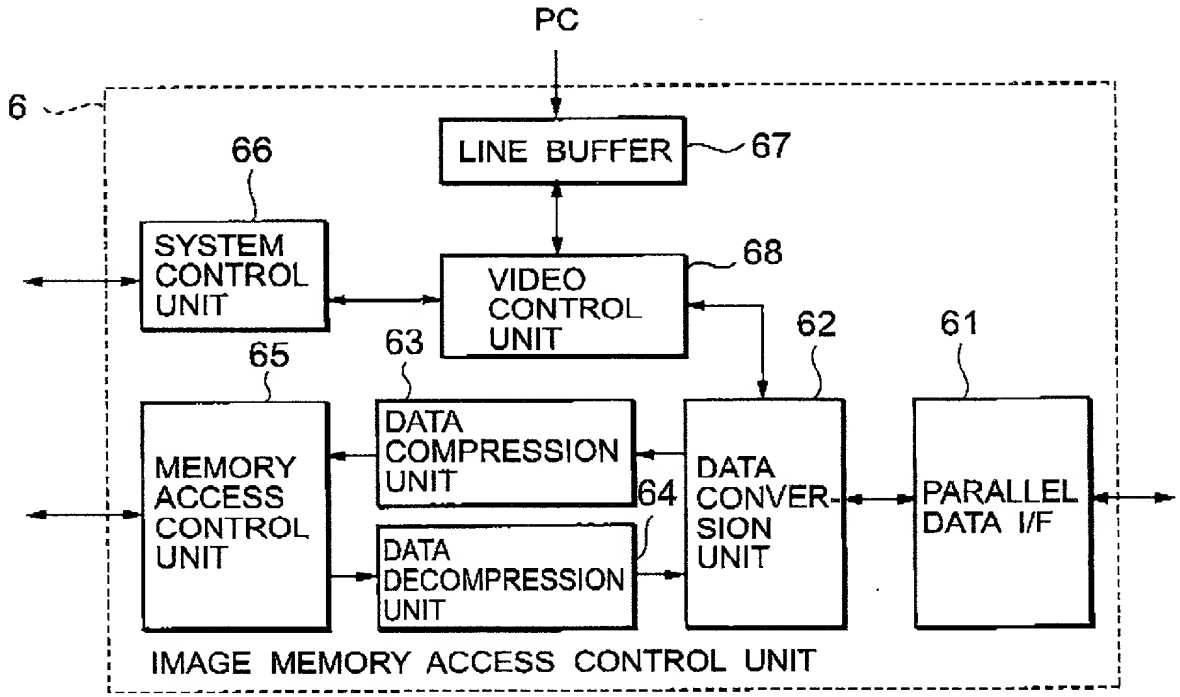

PC
6
66
LINE BUFFER
67
SYSTEM CONTROL UNIT
VIDEO CONTROL UNIT
68
62
61
65
63
DATA COMPRESSION UNIT
MEMORY ACCESS CONTROL UNIT
64
DATA CONVER-SION UNIT
PARALLEL DATA I/F
DATA DECOMPRESSION UNIT
IMAGE MEMORY ACCESS CONTROL UNIT

FIG.5

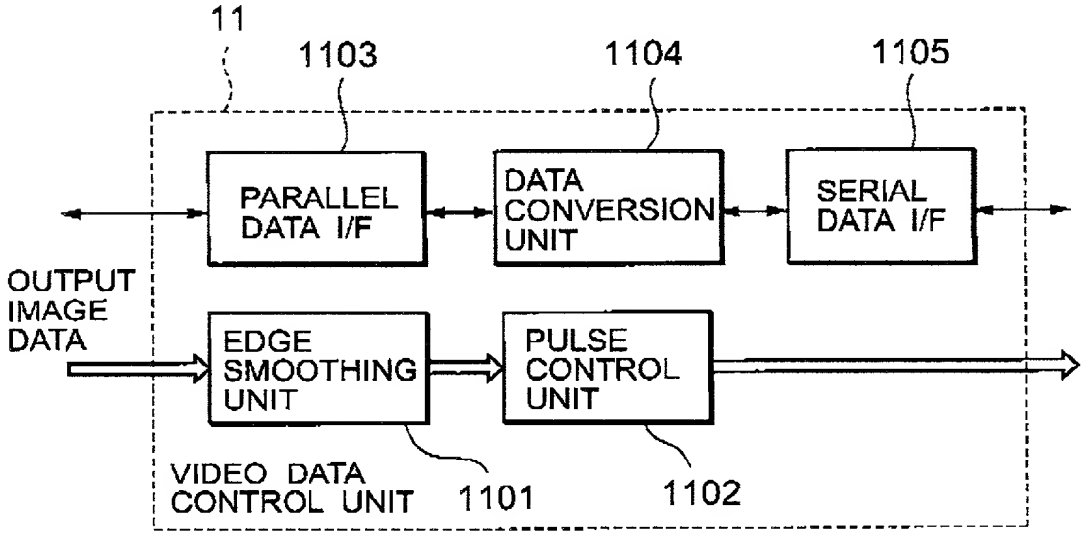
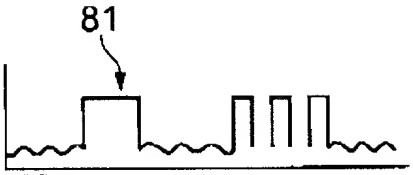

11
1103
1104
1105
PARALLEL DATA I/F
DATA CONVERSION UNIT
SERIAL DATA I/F
OUTPUT IMAGE DATA
EDGE SMOOTHING UNIT
PULSE CONTROL UNIT
VIDEO DATA CONTROL UNIT
1101
1102

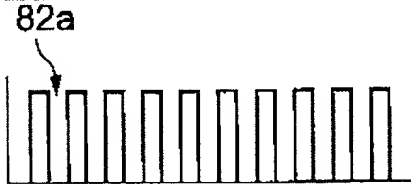
FIG.6

FIG.7A



FRONT IMAGE

FIG.7B1

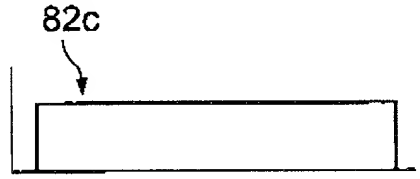


BACK IMAGE
(DOT PATTERN)

FIG.7B2

BACK IMAGE
(CHARACTER)

FIG.7B3



BACK IMAGE
(THICK)

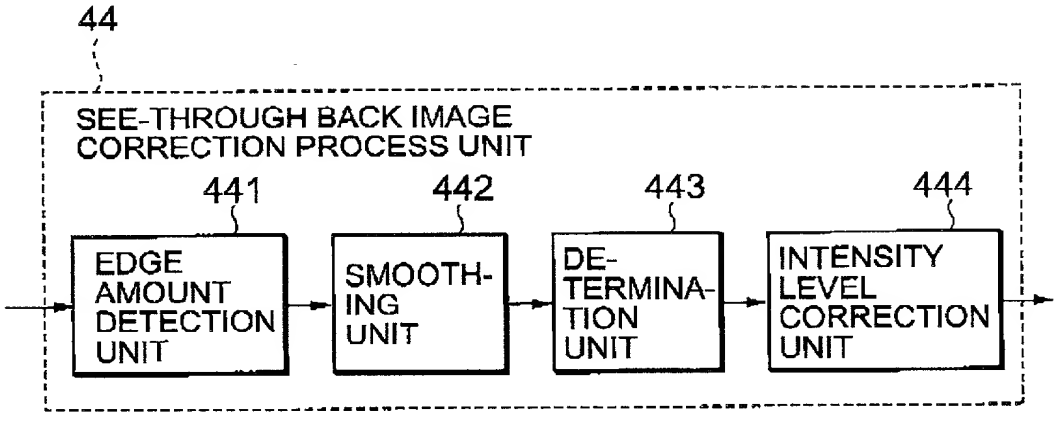


FIG.8

$$L1=\begin{bmatrix} -1 \\ -1+4-1 \\ -1 \end{bmatrix}$$

FIG.9

FIG.10A

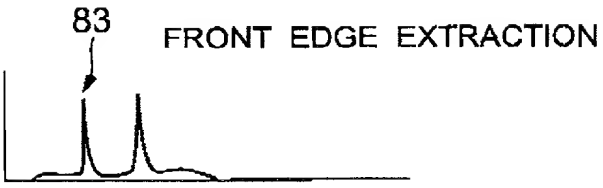


FIG.10B

$$L2=\begin{bmatrix} 1&1&1&1&1 \\ 1&1&1&1&1 \\ 1&1&2&1&1 \\ 1&1&1&1&1 \\ 1&1&1&1&1 \end{bmatrix} X\ 1/26$$

FIG.11

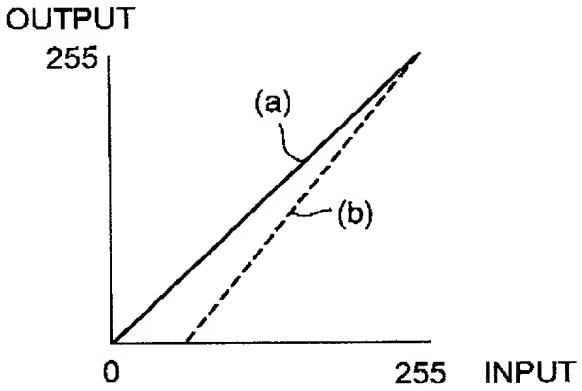
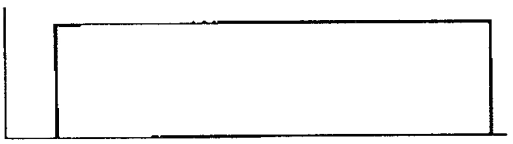


FIG.12

FIG.13A

FIG.13B



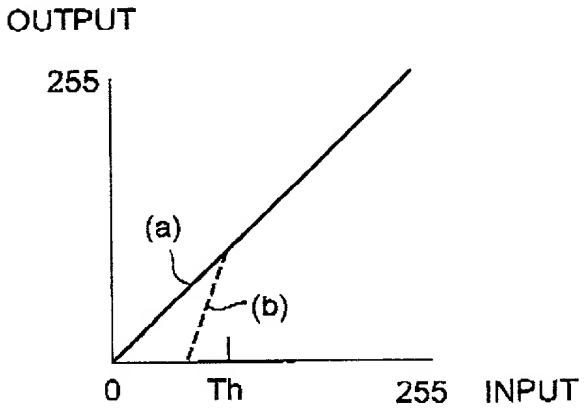


FIG.14

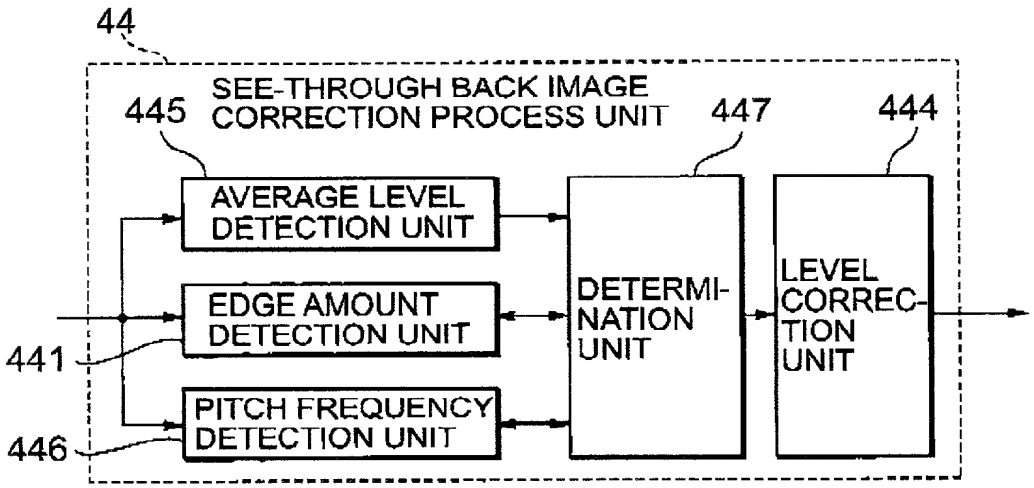

44
SEE-THROUGH BACK IMAGE CORRECTION PROCESS UNIT
445
447
444
AVERAGE LEVEL DETECTION UNIT
EDGE AMOUNT DETECTION UNIT
PITCH FREQUENCY DETECTION UNIT
441
446
DETERMI-NATION UNIT
LEVEL CORREC-TION UNIT

FIG.15

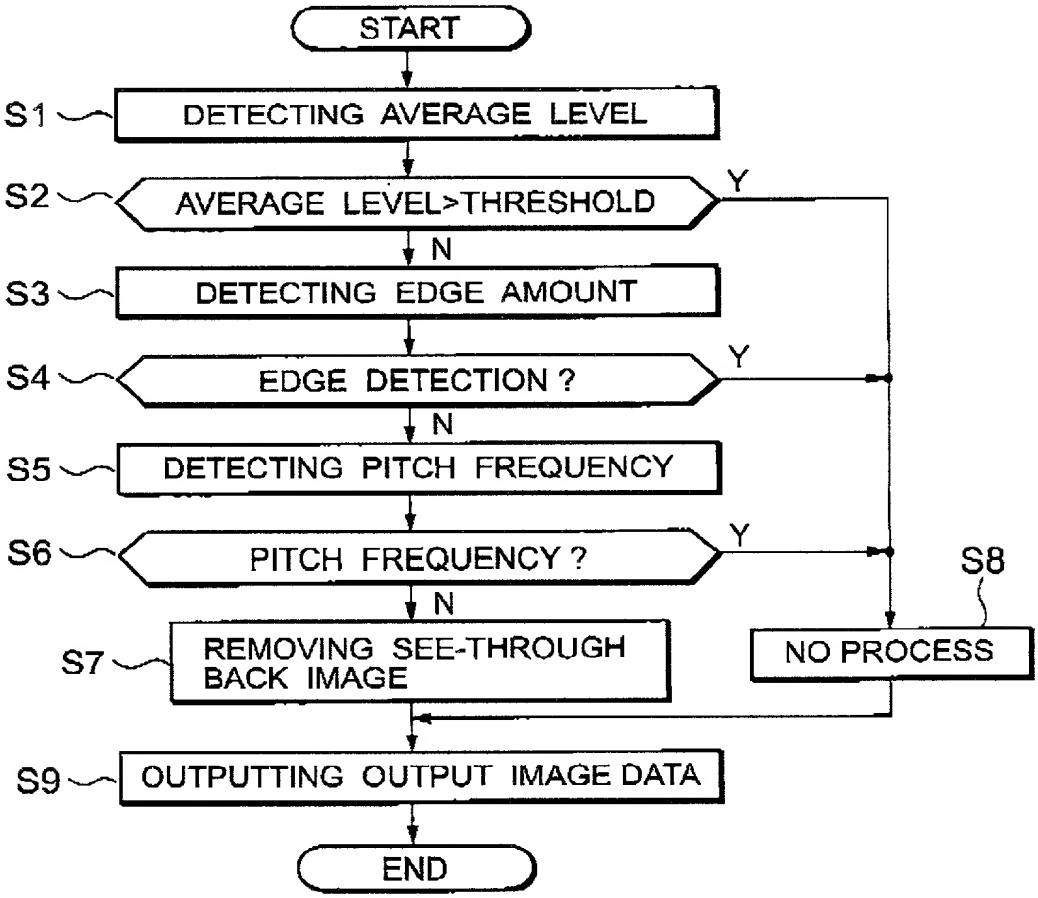
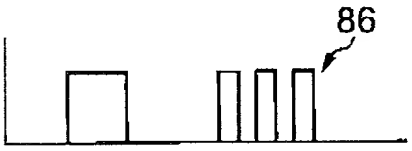

START
S1
DETECTING AVERAGE LEVEL
S2
AVERAGE LEVEL>THRESHOLD
Y
N
S3
DETECTING EDGE AMOUNT
S4
EDGE DETECTION ?
Y
N
S5
DETECTING PITCH FREQUENCY
S6
PITCH FREQUENCY ?
Y
N
S7
REMOVING SEE-THROUGH BACK IMAGE
S8
NO PROCESS
S9
OUTPUTTING OUTPUT IMAGE DATA
END

FIG.16

FIG.17A

FRONT DOT PATTERN DETECTION

FIG.17B

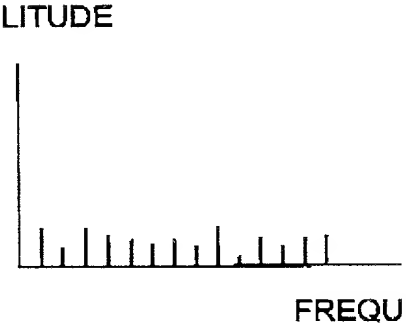


FRONT IMAGE AFTER REMOVING SEE-THROUGH BACK IMAGE

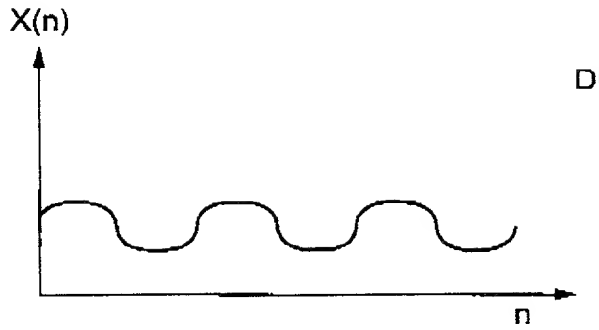
FIG.18A

DOT PATTERN IMAGE

FIG.18B

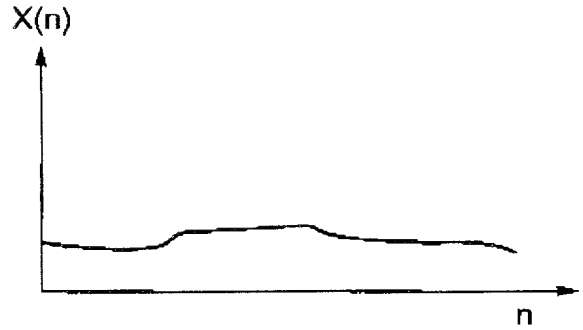


SEE-THROUGH BACK IMAGE



DOT PATTERN IMAGE

FIG.19A



SEE-THROUGH
BACK IMAGE

FIG.19B

M1

D(1,1)	D(1,2)	D(1,3)	D(1,4)	D(1,5)	D(1,6)	D(1,7)	D(1,8)	D(1,9)	· · ·	D(1,N)
D(2,1)	D(2,2)	D(2,3)	D(2,4)	D(2,5)	D(2,6)	D(2,7)	D(2,8)	D(2,9)	· · ·	D(2,N)
D(3,1)	D(3,2)	D(3,3)	D(3,4)	D(3,5)	D(3,6)	D(3,7)	D(3,8)	D(3,9)	· · ·	D(3,N)

D(1,1)	D(1,2)	D(1,3)
D(2,1)	D(2,2)	D(2,3)
D(3,1)	D(3,2)	D(3,3)

M2

D(1,2)	D(1,3)	D(1,4)
D(2,2)	D(2,3)	D(2,4)
D(3,2)	D(3,3)	D(3,4)

M3

D(1,3)	D(1,4)	D(1,5)
D(2,3)	D(2,4)	D(2,5)
D(3,3)	D(3,4)	D(3,5)

M4

M(N-1)

D (1,N-2)	D (1,N-1)	D (1,N)
D (2,N-2)	D (2,N-1)	D (2,N)
D (3,N-2)	D (3,N-1)	D (3,N)

FIG.20